

Compiler Freedom in Quantum EDA Circuits

Exactness-preserving ordering of commuting phase terms — a shielded learned policy, strict equal-cost selection, and a measured hardware boundary

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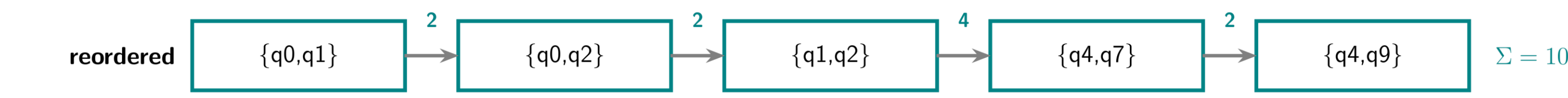
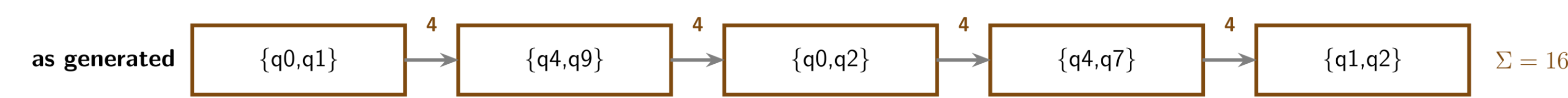
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The freedom

A QAOA cost layer lowers into *commuting* parity terms. Every ordering implements the identical logical operator:

$$\prod_{k=1}^n e^{-i\theta_{O_k} Z_{S_{O_k}}/2} = \prod_{i=1}^n e^{-i\theta_i Z_{S_i}/2}$$

The compiled circuit is not. Order decides which parity work cancels, how far apart supports land on the coupling graph, and how much routing pressure the transpiler carries forward — a **logically free decision with a measurable cost**.



Identical terms and placement; only the visit order differs, so only the transition burden differs.

We freeze a compiler contract — placement, the mapped parity tree for each support, coefficients and provenance, and a clean workspace — so the only remaining freedom is the complete permutation of terms. A candidate failing any check is rejected, never repaired: every routed-cost difference is attributable to the compiler, not to a different circuit.

Two searches

A. Shielded reinforcement learning

A feasibility shield restricts each step to un-emitted terms, so every trajectory is a valid permutation by construction: correctness is a property of the action set, not of the learned weights.

$$\mathcal{A}(s) = R(s), \quad \pi(a \mid s) = 0 \quad \forall a \notin R(s)$$

A linear policy over seven per-action features is trained by an elite (cross-entropy) update against a route-charged proxy:

$$c(t_i \mid S_{\text{prev}}) = |S_i \triangle S_{\text{prev}}| + 0.35 \text{MST}(\phi(S_i)) + 0.15 \text{bridge}(\phi(S_{\text{prev}}), \phi(S_i))$$

B. Plateau-constrained optimization

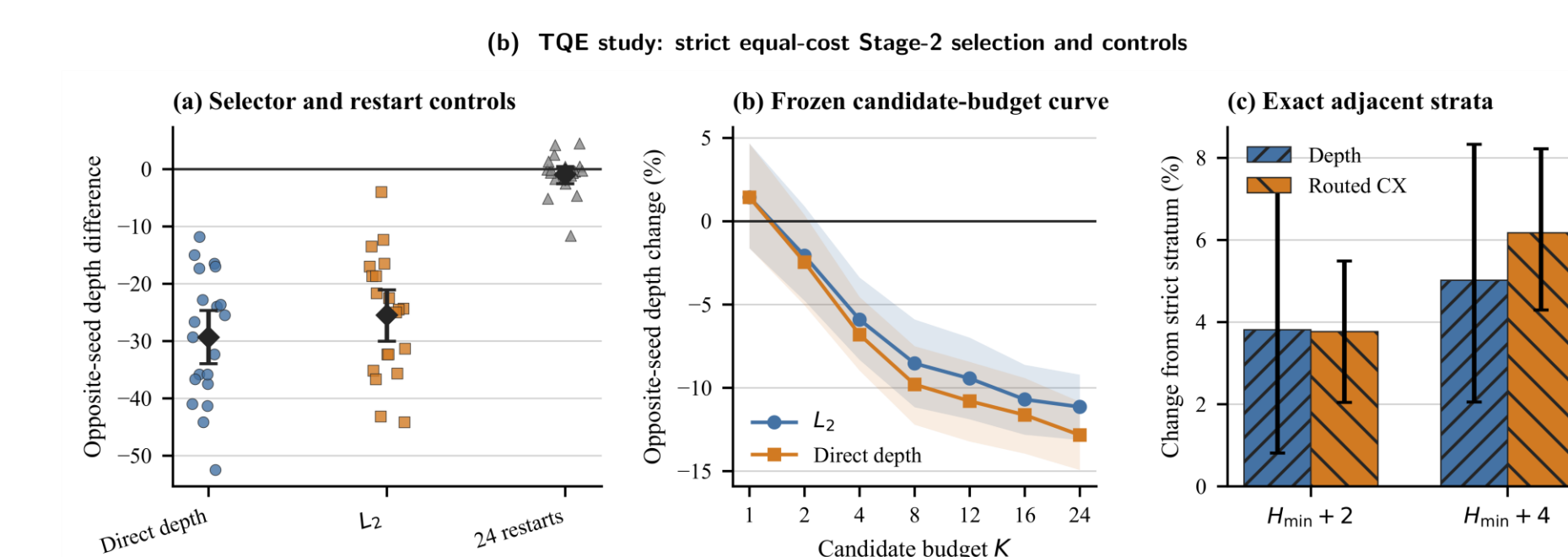
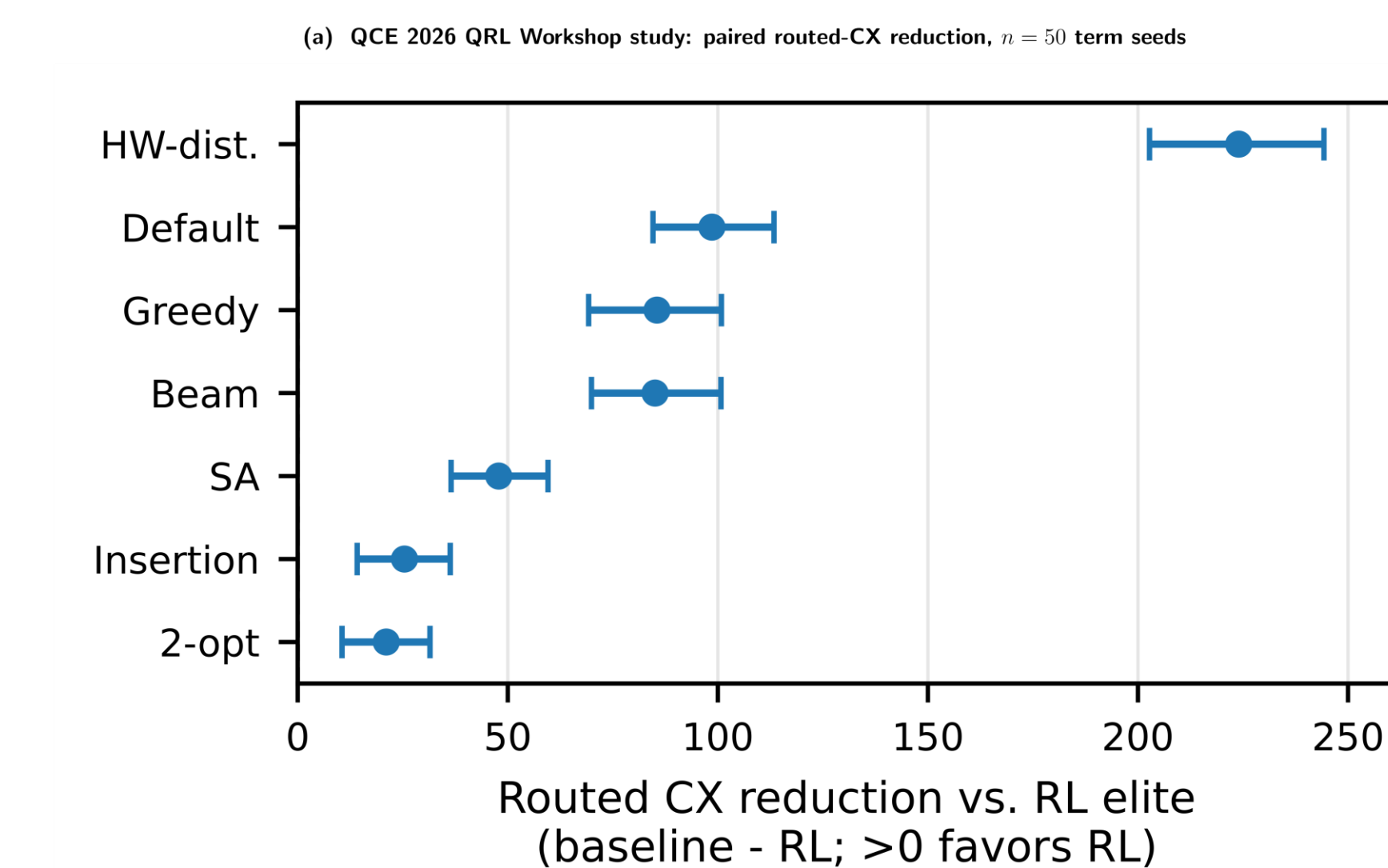
Stage 1 minimizes the coarse support-transition cost. Exact counting then shows that its optimum can contain many tours; Stage 2 searches only inside that certified optimum and selects by training-route depth:

$$O^{(1)} \in \arg \min_O H_{\text{closed}}(O),$$

$$O^{(2)} \in \arg \min_{O: H_{\text{closed}}(O)=H_{\min}} D_{\text{train}}(O)$$

OR-Tools supplies the practical Stage-1 tour; LKH-3 and Held–Karp audit optimization. Stage 2 keeps H_{closed} unchanged by construction; routed depth and CX remain downstream outcomes.

Headline results



Separate protocols, never pooled. (a) Baseline – RL per term seed with Bonferroni-adjusted 95% bootstrap intervals. (b) Stage-2 selector, candidate-budget, and adjacent-stratum controls; negative depth differences favour selection. These compiler results are SABRE-conditioned.

Result I · accepted paper

IEEE International Conference on Quantum Computing and Engineering (QCE) 2026 — Quantum Reinforcement Learning Workshop · accepted [1]

336.0 **-22.3%** **-33.9%**
MEAN ROUTED CX PAIRED CX PAIRED DEPTH

36-term parity-walk components on a synthetic heavy-hex map; 50 term seeds × 2 transpiler seeds, with the *term seed* as the statistical unit.

- Lowest mean routed CX and depth of every tested policy, against the 434.6-CX unoptimized construction order.
- All seven one-sided Wilcoxon comparisons survive Bonferroni correction; routed depth survives as well.
- It also beat warm-started 2-opt and simulated annealing at equal or greater search budget, by 5.7–12.2% paired CX.

Honest boundary. Transfer audits show the proxy is predictive for this component but not for extraction-heavy or token/permutation circuits, which need architecture-aware rewards.

Result II · IEEE TQE journal extension

IEEE Transactions on Quantum Engineering · under review [2]

≥24 **-9.14%** **-12.83%**
EQUAL-COST TOURS / BANK STAGE 1 ROUTED CX STAGE 2 CROSS-SEED DEPTH

Stage 1. At 36 terms, OR-Tools ordering cuts routed CX by 9.14% against the generated order on 20/20 term-seed units. Exact counting through 20 terms separately establishes instance-dependent optimum multiplicity; the middle registered 20-term count is 59,426 tours.

Stage 2. Every 36-term bank supplied 24 sampled tours at the same certified optimum, $H_{\text{closed}} = 74$. The selector never relaxes that primary cost:

$$H_{\text{closed}}(O) = 2n + 2 + 2k, \quad k \in \{0, \dots, n-1\}$$

Direct training-route selection cuts opposite-SABRE-seed depth 12.83% on 20/20 units; a matched 24-restart control changes depth only –0.41% (unresolved). Uniform, hash, and 1,000 permuted-score nulls do not reproduce the effect.

Boundary. The benefit transfers to 48 terms and a bounded MaxCut generator, but reverses under BasicSwap. Tested transition surrogates remain unresolved.

Hardware · scope

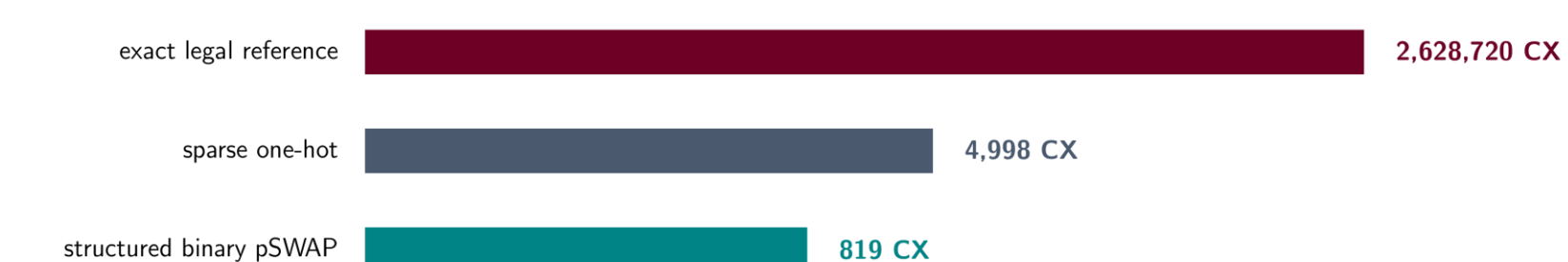
Prospective IBM Heron test. Across 40 term-seed units and 4,096,000 shots, Stage 2 shifted raw stabilizer-generator error from 0.4155 to 0.4130 (–0.0025; –0.59%). The fixed executed panel exceeded shot noise, but the term-seed interval **crossed zero** (24/0/16 favorable/tied/adverse).

This is a small panel-specific hardware observation, not evidence of a general hardware-error reduction.

Earlier Fez, Kingston, and Boston studies remain statistically separate and are never pooled with this prospective test.

Wider architecture

The motivating workload is constraint-preserving QAOA for cell placement. Compressing the legality-preserving mixer by three orders of magnitude moved the bottleneck into the phase separator — now 97.3% of the logical circuit. Manuscript in preparation [3]



Artifacts

github.com/owenfriedewald/shielded-grl · github.com/owenfriedewald/compiler-freedom · doi.org/10.5281/zenodo.22063212 · omfvq4@missouri.edu

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References

- [1] O. Friedewald, A. Shiri Sichani, and C.-R. Shyu, "Shielded RL for route-charged parity-term ordering in QEDA phase components," IEEE Int. Conf. Quantum Computing and Engineering (QCE), Quantum Reinforcement Learning Workshop, 2026 (accepted); arXiv:2607.15307.
- [2] O. Friedewald, A. Shiri Sichani, and C.-R. Shyu, "Plateau-constrained selection of commuting phase-term orderings under a fixed maintained-parity compiler contract," IEEE Trans. Quantum Eng., under review.
- [3] O. Friedewald and A. Shiri Sichani, "Constraint-preserving QAOA for placement: ordering, objective alignment, and circuit realization," manuscript in preparation.